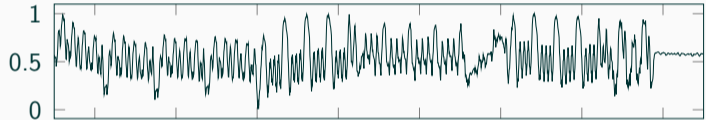


Power Contracts:

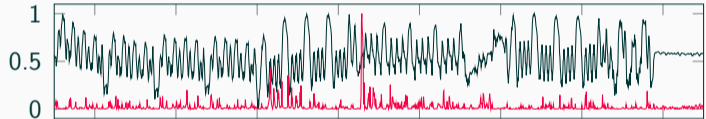
Provably Complete Leakage Models for Processors

Roderick Bloem, Barbara Gigerl, Marc Gourjon,
Vedad Hadžić, Stefan Mangard, Robert Primas

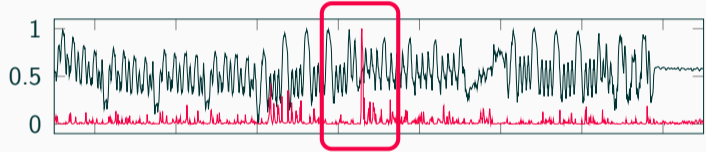
- Processors leak information about processed data through **power side channels**:



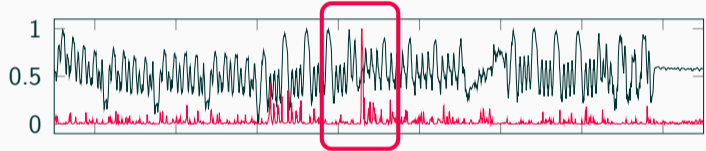
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- Masking** is a side-channel countermeasure
 - Splits secrets into **uniformly random shares**, e.g.,

$$S = S_1 \oplus S_2$$

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xor  x3, x1, x2 ; leaks x1  $\oplus$  x2  
and  x7, x4, x3 ; leaks x4 & x3
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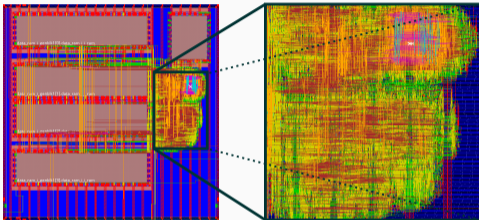
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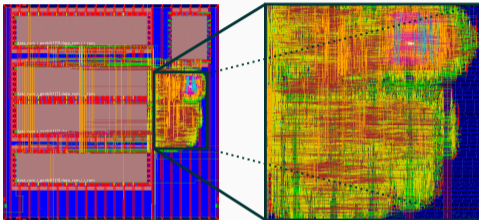
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(Option 2) Verify considering CPU design:

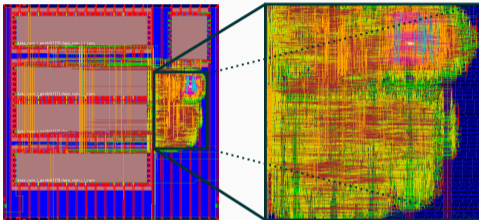




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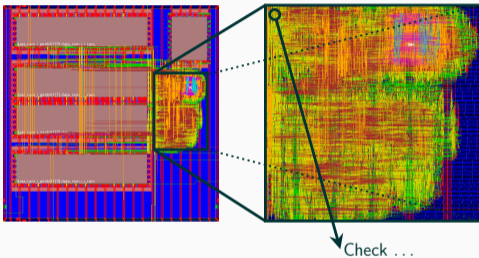
 Complete by definition



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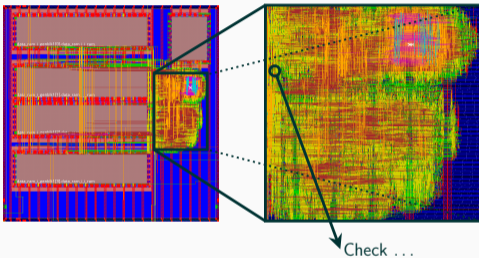
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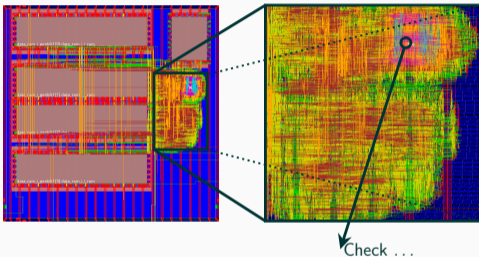
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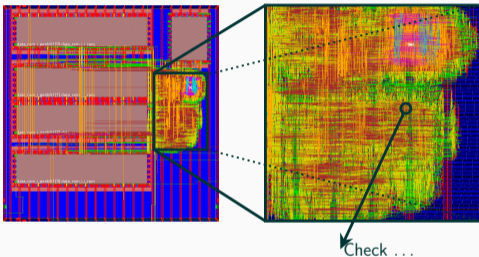
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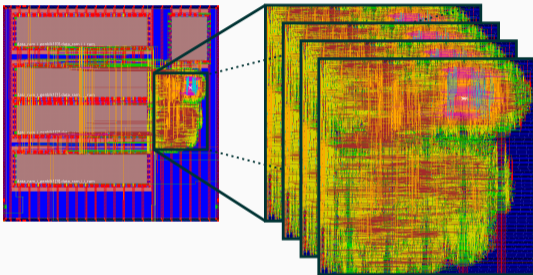
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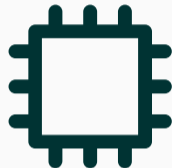
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program



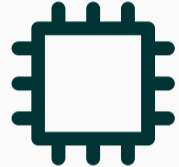
processor



program



contract



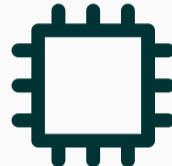
processor



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processor



abstraction layer



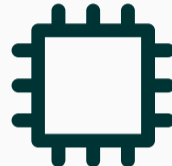
program



contract



Compliant?



processor



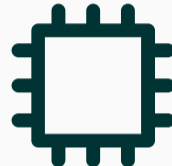
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 completeness





 easy verification





What are Power Contracts?

Contracts **formally** describe a processor.





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- **Functional** (ISA) specification :
 - **architectural** registers, e.g., `pc`, `x1`, `x2`, ...
 - **what** instructions compute, e.g.,

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$$\begin{aligned} \text{xor } x3, x1, x2 &\Rightarrow x3 \leftarrow x1 \oplus x2 \\ &pc \leftarrow pc + 4 \end{aligned}$$

- **Leakage** specification:

- **microarchitectural** elements, e.g., `rf_pA`
- **what** is leaked, e.g., `leak(x1, x2, rf_pA)`



```
1 function clause execute (AND(rs2, rs1, rd)) = {
2   let rs1_val = X(rs1);           // load rs1
3   let rs2_val = X(rs2);           // load rs2
4   let result = rs1_val & rs2_val; // compute
5
6
7
8
9   X(rd) = result;                 // write result
10  pc = pc + 4;                     // update pc
11
12
13  return RETIRE_SUCCESS }
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5   leak(rs1_val, rs2_val);         // ALU leakage
6   leak(rs1_val, rf_pA);           // RF transition rs1
7   leak(rs2_val, rf_pB);           // RF transition rs2
8   leak(X(rd), result);           // WB transition
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11  rf_pA = rs1_val;                 // update RF A port
12  rf_pB = rs2_val;                 // update RF B port
13  return RETIRE_SUCCESS }
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A processor complies with a contract if:

1. They are functionally **equivalent***
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- `leak(x1)` and `leak(x2)`
- `leak(x1 + x2)` and `leak(x1 & x2)`
- **any** other function `g(x1, x2)`

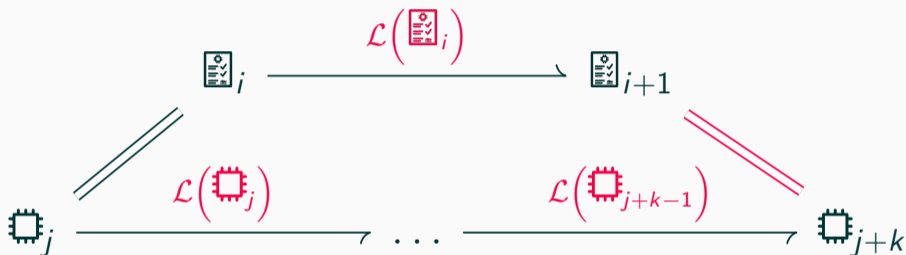








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2. $\exists f_\lambda : \forall \mathbb{C}_j, \mathbb{I}_i : \mathbb{C}_j \simeq \mathbb{I}_i \Rightarrow f_\lambda \circ \lambda(\mathbb{I}_i) = \lambda_g(\mathbb{C}_{l-1}, \mathbb{C}_l)$

We need to show λ is **stronger** than λ_g :

$$\exists f_\lambda : \forall \text{chip}_j, \text{mem}_i :$$

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$$\exists f_\lambda : \forall \text{circuit}_j, \text{mem}_i :$$

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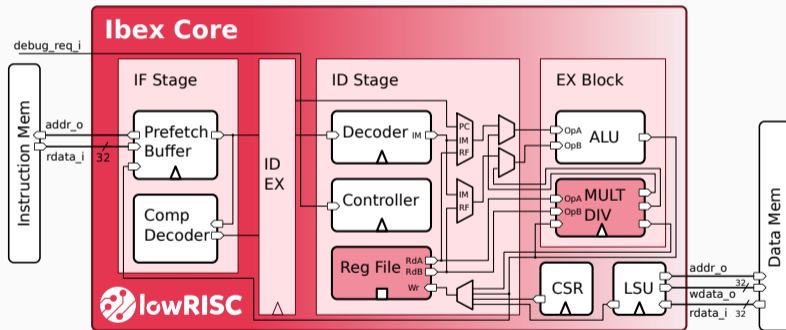
We show it implicitly through congruence:

$$\forall \text{circuit}_j, \text{circuit}'_j, \text{mem}_i, \text{mem}'_i :$$

$$\text{circuit}_j \simeq \text{mem}_i \wedge \text{circuit}'_j \simeq \text{mem}'_i \wedge \lambda(\text{mem}_i) = \lambda(\text{mem}'_i) \Rightarrow$$

$$\lambda_g(\text{circuit}_{l-1}, \text{circuit}_l) = \lambda_g(\text{circuit}'_{l-1}, \text{circuit}'_l)$$

We have created a contract for IBEX:





Almost **all instructions** have the same leakage:

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leak(rs1_val, rs2_val, rf_pA, rf_pB,  
mem_last_addr, mem_last_read);
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Additionally, the writeback stage leaks:

```
leak(x1_val, x1_nval);  
leak(x2_val, x2_nval); //...
```


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- Configuration requires ~ 400 lines
- Compliance verification takes **30.6 hours**



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Gadget	# Instr.	# Clear.	Verification time	
			Contract	Netlist
AND	62	10	< 1 s ✓	284.63 s ✓
Refresh	19	0	< 1 s ✓	32.85 s ✓
XOR	16	1	< 1 s ✓	50.79 s ✓
NOT	5	0	< 1 s ✓	63.32 s ✓



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